

In re the Application of: FLETCHER, Thomas

Director of the U.S. Patent and Trademark Office

Application No.: 09/893,868

Group Art Unit: 2819

Examiner: Not assigned

Washington, D.C. 20231

Filed: June 29, 2001

CASCADED DOMINO FOUR-TO-TWO REDUCER CIRCUIT AND METHOD For:

## INFORMATION DISCLOSURE STATEMENT

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Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The paragraphs marked below are applicable.

- This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date or the date of filing a CPA, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.
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Disclosure Statement was cited in a communication from a foreign patent officing in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more that three months prior to the filing of this Information Disclosure Statement. 37 CF §1.97(e)(2).
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Respectfully submitted,

**KENYON & KENYON** 

Date: F69 28,20.2

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FEB 2 8 2002 INFORMATION BUSCLOSURE STATEMENT BY APPL

09/893,868 **Application Number** June 29, 2001 Filing Date FLETCHER, Thomas First Named Inventor

Not assigned

2819

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2207/11272 Attorney Docket Number

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			U.S. PATENT DO	DCUMENTS		
Examiner Initials *	Cite No.1	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where	
		Number - Kind Code <sup>2</sup> ( <i>if known</i> )			Relevant Passages or Releva Figures Appear	
		6,208,907 B1	03/27/2002	DURHAM et al		

Group Art Unit

**Examiner Name** 

FOREIGN PATENT DOCUMENTS						
Examin er Initials*	Cite No.1	Foreign Patent Document	Publication Date MM-DD- YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				
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OTHER PRIOR ART NON PATENT LITERATURE DOCUMENTS				
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		Yee et al, "Clock-Delayed Domino for Dynamic Circuit Design", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 4, August 2000, pp 425-430		
		Yee et al, "Clock-Delayed Domino for Adder and Combinational Logic Design", IEEE, 1063-6404/96, pp 332-337, 1996		
		Jung, Perepelitsa, Sobelman, "Time Borrowing in High-Speed Functional Units Using Skew-Tolerant Domino Circuits," Proceedings, IEEE International Symposium on Circuits and Systems, pp. V-641 - V-644, 2000		
		Presentation by Carl Sechen dated March 17, 2000.		
		Taub, <i>Digital Circuits and Microprocessors</i> , pages 205-212, McGraw-Hill, 1982		

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Examiner		Date	
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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